REMARKS

Claims 1-3, 5-7, 9, 10 and 12-14 are pending in the present application. Claim 5 has been amended.

Claim Rejections-35 U.S.C. 103

Claims 5-7 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (APA) in view of the Yamaji et al. reference (U.S. Patent No. 6,198,165). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The chip-size semiconductor package of claim 5 includes in combination a connecting portion "directly between the conductive wiring pattern and the conductive post, the connecting portion having a width that gradually decreases from a first boundary at the conductive post to a second boundary at the conductive wiring pattern"; and a dummy pattern "arranged adjacent the first and second boundaries and along sides of the connecting portion, the molding resin also being formed on the dummy pattern". Applicant respectfully submits that the chip-size semiconductor package of claim 5 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

Initially, as described in paragraph [0003] beginning on page 1 of the present application, in conventional chip-size packages, a connecting portion (boundary portion) between a conductive post and a wiring pattern is extremely narrow and weak. The

connecting portion may be broken by stress, which is generated when the molding resin thereon is expanded or contracted.

In an embodiment of the present application as described in paragraph [0026] with respect to Fig. 6, dummy patterns 350 are provided so that stress between the molding resin and connecting portion 340 is dispersed, so that the molding resin may be in good contact and bonded to conductive post 320 and conductive wiring pattern 318. Accordingly, dummy patterns 350 having molding resin thereon, disperse stress between connecting portion 340 and the molding resin thereon.

The Examiner has relied upon Applicant's admitted prior art Figs. 1-4 as showing all the features of claim 5, except for the dummy patterns. In order to overcome this acknowledged deficiency of Applicant's admitted prior art, the Examiner has alleged that it would have been obvious to use dummy wiring patterns 14 as illustrated in Figs. 1 and 2 of the Yamaji et al. reference in the structures as illustrated in Applicant's admitted prior art Figs. 1-4. Applicant respectfully disagrees for the following reasons.

The dummy pattern of claim 5 is featured as "arranged adjacent to first and second boundaries and along sides of the connecting portion, the molding resin also being formed on the dummy pattern". As noted above, since the dummy patterns are provided along side the connecting portion and the conductive wiring pattern with the molding resin thereon, stress between the molding resin and the connecting portion may be dispersed.

One of ordinary skill, looking to reduce stress between molding resin and

respective connecting portions 40 and 140 in Figs. 3 and 4 of Applicant's admitted prior art, would have no motivation to modify the corresponding structures to include dummy patterns in view of the Yamaji et al. reference as asserted by the Examiner. Particularly, as may be readily understood in view of Fig. 1 of the Yamaji et al. reference, **solder resist 7** is formed on dummy wiring patterns 14. As described beginning in column 6, line 64 of the Yamaji et al. reference, by providing the dummy wiring pattern 14 between the pattern of the wiring pattern 8 provided on the surface of insulating substrate 6, the concave portion on the surface of solder resist 7 formed on insulating substrate 6 and wiring pattern 8 becomes less prominent, therefore substantially leveling the surface of solder resist 7.

Accordingly, dummy wiring patterns 14 in the Yamaji et al. reference as relied upon by the Examiner, are merely for the purpose of leveling the surface of solder resist 7 as formed on wiring pattern 8. Dummy wiring patterns 14 do not disperse stress between molding resin and a connecting portion. This should be clear, because solder resist 7 (not molding resin) is formed on dummy wiring patterns 14 and wiring pattern 8 in the Yamaji et al. reference. Accordingly, one of ordinary skill looking to disperse stress between molding resin and respective connecting portions 40 and 140 in Applicant's admitted prior art Figs. 3 and 4, would have no motivation to modify the corresponding structures to include dummy wiring patterns in view of the Yamaji et al. reference, because the dummy patterns of the Yamaji et al. reference do not relieve stress. Applicant therefore respectfully submits that the chip-size semiconductor

package of claim 5 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 5-7, is improper for at least reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 1-3, 9, 10 and 12-14 are allowed.

Conclusion

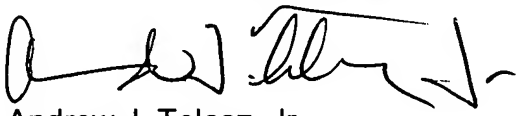
The Examiner is respectfully requested to reconsider and withdraw the above noted rejection, and to pass all the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.
Registration No. 33,581

One Freedom Square
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (703) 715-0870
Facsimile No.: (703) 715-0877